

What is claimed is:

1. A method of making a semiconductor device, comprising:
providing a semiconductor-on-insulator (SOI) wafer having a surface
5 semiconductor layer and a bulk semiconductor layer with a buried insulator layer
therebetween;
thinning at least a portion of the bulk semiconductor layer of the SOI
wafer, thereby producing a thinned portion of the bulk semiconductor layer; and
forming a thermoelectric cooler on a back side of the thinned portion of the
10 bulk semiconductor layer.
2. The method of claim 1, wherein the forming the thermoelectric cooler
includes:
depositing a layer of metal on the back side; and
15 forming at least one pair of semiconductor material blocks on a second
major surface of the metal layer, wherein the semiconductor material blocks have
respective opposite conductivities.
3. The method of claim 2, wherein the forming the semiconductor material
20 blocks includes:
depositing a layer of semiconductor material;
placing an elastomer mask against the layer of semiconductor material;
and
selectively etching the layer of semiconductor material through openings
25 in the elastomer mask.
4. The method of claim 2, wherein the semiconductor material blocks
have respective opposite conductivities.
- 30 5. The method of claim 2, wherein the metal layer has a thickness from
0.5 μm to 50 μm .

6. The method of claim 2, wherein the metal layer has a thickness from 1 μm to 10 μm .

7. The method of claim 2, wherein the metal layer includes silicon
5 germanium.

8. The method of claim 2, wherein the forming the thermoelectric cooler further includes coupling a pair of the semiconductor material blocks to a current source.

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9. The method of claim 2, wherein the forming the semiconductor material blocks includes:

depositing a layer of insulating material;

forming channels in the insulating material at desired locations for the

15 semiconductor blocks; and

depositing semiconductor material in the channels.

10. The method of claim 9, wherein the forming the channels includes uncovering portions of the metal layer.

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11. The method of claim 9, wherein the forming the channels includes etching portions of the insulating material to form the channels.

12. The method of claim 9, wherein the forming further includes reducing
25 thickness of the insulating material and the semiconductor material.

13. The method of claim 12, wherein the reducing thickness includes polishing the insulating material and the semiconductor material.

14. The method of claim 1, wherein the thinning the bulk semiconductor layer is a selective partial thinning, leaving unthinned portions of the bulk semiconductor layer.

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15. The method of claim 1, wherein the thinning includes:
performing a first etch on the at least a portion of the bulk semiconductor
layer, the first etch being performed down to an etch stop;
removing an exposed portion of the etch stop; and
5 performing a second etch on the at least a portion of the bulk
semiconductor layer, to thereby form the thinned portion of the bulk
semiconductor layer.

16. The method of claim 15, wherein the first etch and the second etch
10 utilize different etchants.

17. The method of claim 15, further comprising, prior to the thinning,
forming the etch stop by implanting.

18. The method of claim 1, further comprising forming a transistor that is
15 thermally coupled to the thermoelectric cooler.

19. The method of claim 18, wherein the transistor is thermally coupled to
the thermoelectric cooler through a front side of the thinner portion.
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